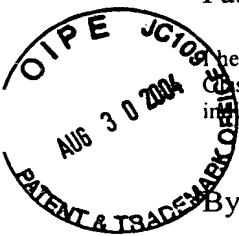


Patent No.: 6,438,053



hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

By: 

Date: August 26, 2004

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12/IDS.
G. Stuby
9-20-04

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent No. : 6,438,053
Patentee : Peter Pöchmüller
Issue Date : August 20, 2002
Title : Integrated Memory Having Memory Cells and Reference Cells
Customer No.: 24131

Hon. Commissioner for Patents
Alexandria, VA 22313-1450

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INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. 1.501

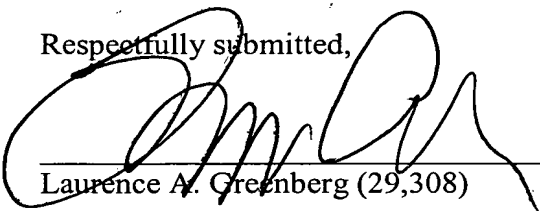
Sir:

In accordance with 37 C.F.R. 1.501, a copy of the following publication is submitted herewith:

Masashi Horiguchi, et al.: "A Flexible Redundancy Technique for High-Density DRAM's",
8107 IEEE Journal of Solid-State Circuits, Volume 26, No. 1, New York, 1991.

It is believed that the enclosed prior art is less pertinent than the prior art previously submitted or cited by the Examiner. It is respectfully requested that the references merely be placed in the PTO file.

Respectfully submitted,


Laurence A. Greenberg (29,308)

Date: August 26, 2004

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